08-07-02

AF/2813

PATENT

Attorney Docket No.: 002818/PDD/PSI/JW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	) Group:
	) Art Unit: 2813
Suketu A. Parikh	) Examiner: Pham T.
	)
Serial No.: 09/244,788	) **TRANSMITTAL LETTER**
	) **APPEAL BRIEF**
Filed: 2/5/99	)
	) PATENT COUNSEL
For: Dual Damascene Misalignment Tolerant Techniques For Vias And Sacrificial Etch Segments	) APPLIED MATERIALS, INC.
	) Legal Affairs Department
	) P.O. Box 450 A
	) Santa Clara, CA 95052

Assistant Commissioner for Patents
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

Sir:

Enclosed for the above-identified application please find:

1. Transmitted herewith in triplicate is the APPEAL BRIEF with respect to the Notice of Appeal filed on March 6, 2002.
2. Fee for filing Appeal Brief $320.00
3. Extension of Term
   Appellant hereby petitions for an extension of time under 37 CFR §1.136 for three (3) months to extend the time to file the enclosed Appeal Brief from two (2) months following the filing of the Notice of Appeal to five (5) months. Based on the extension requested in this petition, the extended period of response will expire on August 6, 2002. If an additional extension of time is required, please consider this a petition therefor.

Certificate Of Mailing Transmission

I hereby certify that this correspondence is being deposited with The United States Postal Service as express mail in an envelope to: Assistant Commissioner for Patens, Washington, D.C. 20231

Express Mail Receipt No. EL263802114US

Date of Deposit August 5, 2002

Signature Beth Mukerji

4. Fee for extension of time for three (3) months $920.00
5. Total fee due:

Appeal Brief fee	$320.00
Time Extension fee	$920.00
TOTAL FEE DUE	$1,240.00

6. **The Commissioner is hereby authorized to charge $1,240.00 to Deposit Account No. 50-1074**
7. **The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1074. A duplicate of this transmittal is enclosed.**

Please address all correspondence to:

PATENT COUNSEL
APPLIED MATERIALS, INC.
Legal Affairs Department
P.O. Box 450 A
Santa Clara, CA 95052

Respectfully submitted,

Dated: 8/5/02

By: _____
Robert W. Mulcahy
Reg. No.: 25,436

PATENT
Attorney Docket No.: 002818/PDD/PSI/JW

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ATTENTION: Board of Patent Appeals and Interferences

Sir:

Appeal Brief

This brief is in furtherance of the Notice of Appeal of March 6, 2002 filed in the above-identified case.

Real Party in Interest

The subject patent application is owned by Applied Materials, Inc. of Santa Clara, California.

Related Appeals and Interferences

There are no related appeals or interferences pending in the subject application.

Status of Claims

Claims 1, 5-13, 15-19 and 23-30 are the subject of this appeal. Claims 2-4, 14, 20-22, 31 and 32 were previously cancelled. Claims 33-42 were previously withdrawn from consideration, since these claims were drawn to a nonelected invention. There are no allowed claims.

Status of Amendments

On December 18, 2001 appellant filed an amendment in response to the FINAL ACTION dated 10/18/01. Claims 5, 11-13, 15, 19 and 24 are amended in the 10/18/01 amendment. The Examiner refused to enter the 10/18/01 amendment for "raising new issues that require further search/consideration", as stated in the ADVISORY ACTION mailed on 1/15/02.

Summary of Invention

A first group of embodiments of the subject invention is pertinent to claims 1 and 5-12 regarding methods for forming a structure on a substrate wherein a via pattern is employed that is wider than he overlaying trench pattern. Independent method claim 1 provides the limitations of depositing a first dielectric layer on a substrate, followed by sequentially depositing a second dielectric layer and a first mask layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics (specification at page 10, lines 1-18 and Fig. 5A). As recited in claim 1, a first via pattern is formed in the first mask layer, this pattern is then etched through the second dielectric layer forming a second via pattern, after which the first etch mask layer is removed and a third dielectric layer is deposited, such that the second and third dielectric layers comprise materials having dissimilar etching characteristics, whereafter a second etch mask layer is deposited on the third dielectric layer (specification at page 10, line 20 through page 11, line 12 and Figs. 5C-5E). Continuing the present invention as recited in claim 1, a trench pattern is formed in the second etch mask layer, such that (1) the trench pattern overlays the first via pattern and (2) the width of the first via pattern exceeds the width of the trench pattern. The trench pattern is then etched through the third dielectric layer, thereby forming (1) a first trench in the third dielectric layer and (2) a second via

pattern (specification at page 11, lines 14-28 and Figs. 5F-5G). The second via pattern is then etched through the first dielectric layer thereby forming a via hole to the substrate, and a second trench is formed by etching the first trench through the second dielectric layer (specification at page 11, line 30 through page 12, line 6 and at page 13, lines 1-7, Figs. 5G and 6A). Claim 1 thus recites forming a structure wherein the via hole and trench are adapted for forming a dual damascene structure (specification at page 13, lines 11-14 and fig. 6B). The method of claim 1 can additionally include the limitation that the width of the first via exceeds the width of the trench pattern by at least 0.02 μ, see claim 6 depending from claim 1 (specification at page 10, lines 26-29). The first and third dielectric layers can comprise a group of enumerated dielectric materials as recited in claim 7 depending from claim 1 (specification at page 19, lines 4-21). The second dielectric layer can comprise a group of enumerated dielectric materials as recited in claim 8 depending from claim 7 (specification at page 19, lines 4-21). Furthermore, the mask layers employed in the method of claim 1 can include photoresist , hard mask layers and combinations of photoresist and hard mask layers, see claim 9 depending from claim 1 (specification at page 18, lines 23-26). The first and third dielectric layers can be limited to Black Diamond ™, see claim 10 depending from claim 1 (specification at page 19, lines 23-28). Additionally, the via and trench formed as recited in claim 1 can be filled simultaneously with a conductive material, thereby forming a dual damascene structure, see claim 11 depending from claim 1 (specification at page 13, lines 11-14 and Fig. 6B). Suitable conductive materials for forming the dual damascene structure are recited in claim 12 depending from claim 11 (specification at page 23, lines 9-12). The method as summarized above in connection with claim 1 can further include (1) depositing the first dielectric layer on the substrate such that there is no material layer interposed between the interconnect line and the substrate, and (2) such that the first and third dielectric layers comprise materials having similar etching characteristics, see independent claim 5 (specification at page 10, line 5 through page 12, line 9 and Figs. 5A-5H).

A second group of embodiments of the subject invention is pertinent to claims 13, 15-19 and 23-30 regarding methods for fabricating a dielectric stack employing an etch

stop layer wherein a portion of the etch stop layer is removed to form a sacrificial etch segment. Independent method claim 13 provides limitations including forming a dielectric stack including an etch stop layer and depositing a first mask layer on the etch stop such that the first mask layer includes first and second via patterns and a sacrificial etch pattern positioned between the via patterns, whereafter the via patterns are etched through the etch stop layer and also etching the sacrificial etch pattern through the etch stop layer to form a sacrificial etch segment (specification at page 14 lines 12-29 and Figs. 8A-8C). A first and a second trench are formed on the etch stop layer such that the trenches (1) do not overlay the sacrificial etch segment, (2) the sacrificial etch segment is positioned between the trenches, (3) the distance between the trenches exceeds the width of the sacrificial etch segment and (4) and the width of the first via pattern exceeds the width of the first trench while the width of the second via pattern exceeds the width of the second trench (specification at page 14, line 31 through page 15, line 13, at page 15 line 31 through page 16, line 16 and Figs. 8D-8F). First and second via holes are then formed such that the first via hole underlies the first trench and the second via hole underlies the second trench wherein the first via and first trench, and the second via hole and second trench are adapted for forming first and second dual damascene structures (specification at page 15 line 10-16 and Figs. 8F-8G). The method of claim 13 can include the limitations wherein the distance between the first and second trenches exceeds the width of the sacrificial etch pattern by at least 0.02 μ, see claim 15 depending claim 13 (specification at page 16 lines 10-18). The etch stop layer can comprise a group of enumerated dielectric materials as recited in claim 16 depending from claim 13 (specification at page 17, lines 18-20 and page 19 lines 6-9). Additionally, the vias and trenches formed as recited in claim 13 can be filled simultaneously with a conductive material thereby forming dual damascene structures, see claim 17 depending from claim 13 (specification at page 15 lines 14-17 and Fig. 8G). Suitable conductive materials for forming the dual damascene structures are recited in claim 18 depending from claim 17 (specification at page 23, lines 4-12). Independent method claim 19 provides forming a structure on substrate including the limitations of depositing a first dielectric layer on a substrate and then forming a second dielectric layer on the first dielectric, wherein the first and second dielectric layers comprise materials having dissimilar etching

characteristics. Subsequently, a first mask layer is formed on the second dielectric layer wherein the first mask layer includes first and second via patterns and a sacrificial etch pattern positioned between the via patterns (specification at page 14, lines 12-26 and Figs. 8A-8B). Continuing the present invention as recited in claim 19, the via patterns are etched through second dielectric layer while the sacrificial etch pattern is simultaneously etched through the second dielectric layer thus forming a sacrificial etch segment, after which the first etch mask layer is removed (specification at page 14 line 31 through page 15 line 3 and Fig. 8C). A third dielectric layer is deposited on the second dielectric layer such that the second and third dielectric layers comprise materials having dissimilar etching characteristics, and then a second mask layer is formed on the third dielectric layer such that (1) a first trench pattern overlays the first via pattern while a second trench pattern overlays the second via pattern and (2) the distance between the trench patterns exceeds the width of the sacrificial etch pattern (specification at page 15, lines 3-10 and Figs. 8D-8E). First and second trenches are formed by etching the respective etch patterns through the third dielectric layer, additionally forming third and fourth via patterns by utilizing the first and second etch patterns respectively, whereafter the third and fourth via patterns are etched through the first dielectric layer thereby forming first and second via holes wherein (1) the first via hole and the first trench are adapted for forming a first dual damascene structure and (2) the second trench and second via hole are adapted for forming a second dual damascene structure (specification at page 15, lines 10-16 and Figs. 8F-8G). The method of claim 19 can include a limitation wherein the first and third dielectric layers comprise materials having similar etching characteristics, see claim 23 depending from claim 19 (specification at page 11, lines 6-7 and page 15, lines 13-14). Additionally, the distance between the first and second trenches can exceed the width of the sacrificial etch pattern by at least 0.02 μ, as recited in claim 24 depending from claim 19 (specification at page 16, lines 16-18). The first and third dielectric layers can comprise a group of enumerated dielectric materials, see claim 25 depending from claim 19, while the second dielectric layer can comprise a group of enumerated dielectric materials as recited in claim 26 depending from claim 25 (specification at page 19, lines 4-21). Additionally, the first and third dielectric layers can be limited to Black Diamond ™, see claim 27 depending from claim 19 (specification at

page 19, lines 23-28). Furthermore the first mask layer can include photoresist mask layers, hard mask layers and combinations photoresist and hard mask layers, see claim 28 depending from claim 19 (specification at page 18, lines 23-26). Additionally, the vias and trenches formed as recited in claim 19 can be filled simultaneously with a conductive material thereby forming dual damascene structures, see claim 29 depending from claim 19 (specification at page 15, lines 14-17 and Fig. 8G). Suitable materials for forming the dual damascene structures are recited in claim 30 depending from claim 29 (specification at page 23, lines 4-12).

Issues

Issue 1 – Whether the examination of claim 1 has made out the Patent and Trademark Office's burden for rejecting claim 1 as being obvious to those of ordinary skill in the art?

Issue 2 – Whether the examination of claims 1, 5 and 9 has made out the Patent and Trademark Office's burden of establishing a *prima facie* case for rejecting the patentability of claims 1, 5 and 9 under 35 USC §102(e) as being anticipated by Inohara et al. (U.S. Pat. No. 5,976,972), and whether the examination of claim 19 has made out the Patent and Trademark Office's burden of establishing a *prima facie* case for rejecting claim 19 under 35 USC §102(e) as being anticipated by Lin (U.S. Pat. No. 6,093,632)?

Issue 3 – Whether the examination of claims 6-8, 10, 15 and 24-27 has made out the Patent and Trademark Office's burden of establishing a *prima facie* case for rejecting the patentability of claims 6-8, 10, 15 and 24-27 under 35 USC 103(a) over Lin (U.S. Pat. No. 6,093,632) in view of Inohara et al. (U.S. Pat. No. 5,976,972)?

Issue 4 - Whether claims 1, 5, 7, 8, 11 and 12 are patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972)?

Issue 5 – Whether claims 13 and 16-18 are patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972)?

Issue 6 – Whether claims 13 and 16-18 are patentable under 35 USC §102(e) over Lin (U.S. Pat. No. 6,093,632)?

Issue 7 – Whether claims 19, 23 and 28-30 are patentable under 35 USC §102(e) over Lin (U.S. Pat. No. 6,093,632)?

Issue 8 – Whether claim 11 is patentable under 35 USC §112, second paragraph?

Issue 9 – Whether the proposed amendments of claims 5, 11-13, 15, 19 and 24 raise new issues that require further search/consideration?

Grouping of Claims

For each ground of rejection which appellant contests herein which applies to more than one claim such additional claims, to the extent separately identified and argued below, do not stand or fall together.

The Argument

Issue 1 – Whether the examination of claim 1 has made out the Patent and Trademark Office's burden for rejecting claim 1 as being obvious to those of ordinary skill in the art?

The Examiner's Final Action, Detailed Action memorandum, mailed 10/18/01, item 7 (Response to Arguments), pages 11-12, includes the following statement.

> Regarding to applicant's argument on pages 7-8 that "applicant sequentially forms first and second dielectric layer on a substrate without interposing a cap layer between the first dielectric and the substrate" and Inohara et al teaches "forms the via hole through the first dielectric layer and the cap layer" while "applicant's via hole that extends to the substrate is not formed through a cap layer", the argument is not persuasive because the claim language does not excluding [sic] the step of forming a cap layer (claim 1 uses "the method comprising"). Rejection, therefore, is still proper.

Moreover, forming or not forming a cap layer depending on the design choice of a structure on a substrate is obvious for those skilled in the art. (emphasis added).

Appellant notes that the above statement is the Examiner's response to appellant's arguments concerning the rejection of claim 1 under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972). Applicant submits that the above quoted statement concerning "forming or not forming a cap layer depending on design choice of a structure on a substrate is obvious for those skilled in the art" constitutes the Examiner's assertion of an obviousness rejection.

The MPEP §707.07(d) requirements for claim rejection include:

1. "the ground for the rejection must be fully stated"
2. "the word 'reject' must be used"
3. "The examiner should designate the statutory basis for any ground of rejection by express reference to a section of 35 U.S.C. in the opening sentence of each ground of rejection"

Regarding the MPEP requirements, the Examiner failed to fully state the ground for rejection by for example not (1) making reference to one or more prior art publications, where these are used by the Examiner to make the determination, or (2) stating that the rejection is within the Examiner's personal knowledge (37 CFR §1.104(c) and (d)). In the examination, the word "reject" has not been used in connection with obviousness. Also, the 35 U.S.C. statutory basis is not provided in connection with obviousness regarding the above Examiner's statement.

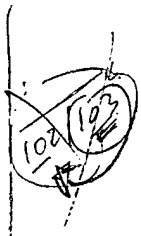
For the reasons provided above, appellant believes that the examination of claim 1 has failed to make out a case for the rejection of claim 1 as being obvious.

Issue 2 – Whether the examination of claims 1, 5 and 9 has made out the Patent and Trademark Office's burden of establishing a prima facie case for rejecting the patentability of claims 1, 5 and 9 under 35 USC 102(e) as being anticipated by Inohara

et al. (U.S. Pat. No. 5,976,972), and whether the examination of claim 19 has made out the Patent and Trademark Office's burden of establishing a prima facie case for rejecting claim 19 under 35 USC §102(e) as being anticipated by Lin (U.S. Pat. No. 6,093,632)?

The Examiner rejected claims 7-9 "under 35 USC 102(e) as being anticipated by Inohara et al [US 5,976,972]", see Final Action, Detailed Action, mailed 10/18/01, item 3, pp. 3,4. The Examiner rejected claim 19 "under U.S.C. 102(e) as being anticipated by Lin [US 6,093,632], see Detailed Action, item 4, pp. 7-9.

A. Regarding claim 1. The Examiner failed to examine the claim 1 limitations "wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics" (clause b), and "wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics" (clause f) under 35 USC §102(e) as being anticipated by Inohara et al. (U.S. Pat. No. 5,976,972).



B. Regarding claim 5. The Examiner failed to examine the claim 5 limitations "wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics" (clause b), and "wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics and wherein the first and third dielectric layers comprise materials having similar etching characteristics" (clause f) under 35 USC §102(e) as being anticipated by Inohara et al. (U.S. Pat. No. 5,976,972).

C. Regarding claim 9. The Examiner failed to examine the claim 9 limitation "The method of claim 1 wherein depositing a first mask layer comprises depositing a mask layer selected from the group consisting of photoresist mask layers, hard mask layers and combinations of photoresist mask layers and hard mask layers" under 35 USC 102(e) as being anticipated by Inohara et al. (U.S. Pat. No. 5,976,972).

D. Regarding claim 19. The Examiner failed to examine the claim 19 limitations "wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics" (clause b), and "wherein the second and third dielectric layers

comprise materials having dissimilar etching characteristics" (clause f) " under 35 USC 102(e) as being anticipated by Lin (U.S. Pat. No. 6,093,632).

The Board of Patent Appeals and Interferences has stated "It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office" *See Ex parte Skinner,* 2 USPQ2d 1788, 1788-1789 (BPAI 1986). The court in *In re Warner and Warner,* 154 USPQ 173, 177 (CCPA 1967) held that the precise language of 35 U.S.C. 102 "clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103". Regarding the examination of all claim limitations: "It is axiomatic that not only must claims be given their broadest reasonable interpretations consistent with the specification, but also that all limitations *must be* considered", *In re Saether,* 181 USPQ 36, 39 (CCPA 1974) (emphasis added). Also, *see In re Lowry,* 32 USPQ2d 1031, 1034 (Fed. Cir. 1994). *"The PTO must* consider all claim limitations when determining patentability of an invention over the prior art". (emphasis added).

Appellant believes that the Examiner has failed to meet the *Ex parte Skinner, In re Warner and Warner, In re Saether* and *In re Lowry* requirements for establishing a *prima facie* case of anticipation regarding claims 1, 5, 9 and 19 under 35 USC §102(e). Appellant therefore believes that the examination of claims 1, 5 and 9 has failed to make out a *prima facie* case for rejecting the patentability of claims 1, 5 and 9 under 35 USC §102(e) as being anticipated by Inohara et al. (U.S. Pat. No. 5,976,972), and that the examination of claim 19 has failed to make out a *prima facie* case for rejecting the patentability of claim 19 under 35 USC §102(e) as being anticipated by Lin (U.S. Pat. No. 6,093,632).

Issue 3 – Whether the examination of claims 6-8, 10, 15 and 24-27 has made out the Patent and Trademark Office's burden of establishing a prima facie case for rejecting the patentability of claims 6-8, 10, 15 and 24-27 under 35 USC 103(a) over Lin (U.S. Pat. No. 6,093,632) in view of Inohara et al (U.S. Pat. No. 5,976,972)?

The Examiner rejected claims 6-8, 10, 15 and 24-27 "under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] in view of Inohara et al. [US 5,976,972]", see Final Action, Detailed Action, item 5, pp. 9-11.

A. Regarding claims 6, 15 and 24. Claims 6 and 15 depend from claim 1, while claim 24 depends from claim 19. Regarding the Examination of claims 6, 15 and 24 for obviousness, the Examiner states:

> "Therefore, one of ordinary skill in the requisite art at the time of [sic] invention was made would have used any suitable range of N or M in the process of Lin *and/or* Inohara et al in order to optimize the process", see Detailed Action at p. 11 (emphasis added).

B. Regarding claims 7, 10, 25 and 27. Claims 7 and 10 depend from claim 1, while claim 25 and 27 depend from claim 19. Regarding the Examination of claims 7, 10, 25 and 27 for obviousness, the Examiner states:

> It would have been obvious for those skilled in the art to use any of these material [sic] in the process of Lin *and/or* Inohara et al to make a dual damascene structure – since it has been well-known in the art that these materials can provide a good dual damascene structure with a decreased capacitance for a better interconnection in a semiconductor device, see Detailed Action at p. 10 (emphasis added).

C. Regarding claims 8 and 26. Claim 8 depends from claim 7, while claim 26 depends from claim 25. The Examiner has failed to provide a specific ground for rejecting claims 8 and 26 under 35 USC §103(a).

The Examiner is required to clearly explain "the pertinence of each reference" when "rejecting claims for want of novelty or obviousness" (CFR §1.104(c) (2)), and to fully and clearly state "the ground of rejection", see MPEP §707.07(d). The Examiner rejected claims 6, 7, 10, 15 and 24-27 over Lin in view of Inohara et al. However, the Examiner then referred to "Lin and/or Inohara et al" in connection with the rejection of these claims, thus failing to clearly state whether the 35 USC §103(a) rejection of claims 6, 7, 10 ,15 and 24-27 is with reference to:

- Lin, or

- Inohara et al., or
- Lin and Inohara et al., or
- over Lin in view of Inohara et al.

Appellant thus believes that the rejection of claims 6-8, 10, 15 and 24-27 under 35 USC §103(a) fails to meet the above cited CFR and MPEP requirements to clearly explain "the pertinence of each reference" and to "fully and clearly state" the ground of rejection.

For the reasons stated above, appellant believes that the examination of claims 6-8, 10, 15 and 24-27 has failed to make out a *prima facie* case for rejecting the patentability of claims 6-8, 10, 15 and 24-27 under 35 USC 103(a) over Lin (U.S. Pat. No. 6,093,632) in view of Inohara et al. (U.S. Pat. No. 5,976,972).

Issue 4 – Whether claims 1, 5, 7, 8, 11 and 12 are patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972)?

A. Regarding claim 1. Independent method claim 1 includes the following limitations in clauses (a) and (i):

a) depositing a first dielectric layer on the substrate

i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the substrate.

Appellant notes that the term "on" as recited in clause (a) has a well defined meaning. See for example *Senmed Inc. v. Richard-Allen Medical Industries Inc.,* 12 USPQ2d 1508, 1512, 1513 (Fed. Cir. 1989) holding that the claim language "on said anvil surface" means "in physical contact with" that surface. Additionally, it is well established that "Words in a claim 'will be given their ordinary and accustomed meaning unless it appears that the inventor used them differently' ". *See Envirotech Corp. v. Al George, Inc.* 221 USPQ 473, 477 (Fed. Cir. 1984), citing with approval *Universal Oil Products Co. v. Globe Oil & Refining Co.,* 54 USPQ 504 (7th Cir. 1943) aff'd 61 USPQ 382

(1944). Regarding the ordinary and accustomed meaning of the term "on", appellant makes reference to the dictionary meaning of this term, stating in part:

> **On . . . *prep.*** **1** in a position above, but in contact with and supported by; upon **2** in contact with (any surface); covering or attached to . . . (see Webster New World Dictionary, Third College Edition, Simon & Schuster, Inc. New York, New York, 1988, p. 946.

In connection with the above dictionary reference appellant notes that the courts have found that "texts such as dictionaries" may be required for claim construction "*C.E. Equipment Co. Inc. v. U.S.*, 13 USPQ2d 1363, 1367 (Cl. Ct. 1989).

In view of the above, appellant respectfully submits the use of term "on" in clause (a) of claim 1 means that the first dielectric layer is in contact with the substrate.

The '972 patent teaches forming a stopper film 54 on the lower wiring element 42 (column 13, lines 6-11 and Fig. 28). The '972 stopper film, when compared with claim 1, constitutes forming a stopper film between appellant's substrate and appellant's first dielectric layer (clause a). Also, the '972 patent discloses as follows.

> As is shown in FIG. 31, those portions of the stopper films 44 and 54, which are exposed to the groove 46 and contact hole 48, are etched away simultaneously, and the lower wiring element 42 is exposed to the bottom of the contact hole 48 (column 13, lines 49-53).

Interposing the '972 cap layer between a layer such as appellant's claimed first dielectric layer and the '972 lower wiring element such as appellant's claimed substrate would result in forming a structure wherein appellant's first dielectric layer is *not deposited on* the substrate. This is contrary to claim 1 wherein the first dielectric layer is formed on the substrate. Additionally, if a cap layer were present between the substrate and the dielectric layer, the clause (i) limitation "etching the second via pattern through the first dielectric layer, *thereby* forming a via hole extending to the substrate" (emphasis added) would be inoperable. Regarding the examination of a patent application the court in *Ex parte Petersen*, 228 USPQ 216, 217 (BPAI 1985) stated "It is axiomatic that not only must claims be given their broadest reasonable interpretation consistent with the specification but also all limitations must be considered". More specifically regarding

claim limitations in connection with the term comprising, the court in *Moleculon Research Corp. v. CBS, Inc.*, 229 USPQ 805, 812 (Fed. Cir. 1986) held "Whether structural recitation limits a claim depends on the language of the claim, the specification, prosecution history, and other claims." Appellant notes that MPEP §2111.03 makes reference to *Moleculon*, with approval, regarding the meaning of the term comprising. In view of *Moleculon*, appellant respectfully submits that clause (a) provides a structural limitation to the term comprising wherein appellant's first dielectric layer is formed such that this layer makes contact with – and is formed on – the substrate.

In view of the reasons provided above, appellant believes that it is inappropriate to construe claim 1 as additionally including the following steps: (1) depositing a cap layer on the substrate, (2) subsequently depositing a first dielectric layer on the cap layer and (3) anisotropically etching the second via pattern through the cap layer.

Anticipation under 35 USC §102 requires identity of invention in a single reference, see for example MPEP §2131. It is well established that the courts apply a rigorous test for a finding of anticipation. "For a prior art reference to anticipate a claim, the reference must disclose each and every element of the claim *with sufficient clarity* to prove its existence in the prior art." *See Motorola Inc. v. Interdigital Corp.,* 43 USPQ2d 1655, 1657 (Fed. Cir. 1990). Furthermore, "[A]ny degree of physical difference, *however slight*, invalidates claims of anticipation. *See E.I. du Pont de Nemours & Co. v. Polaroid Graphics Imaging Inc.* 10 USPQ2d 1579, 1585 (D. Del 1989) (emphasis added), *aff'd* 13 USPQ2d 1731 (Fed. Cir. 1989). Also, "[T]here is no anticipation 'unless all of the elements are found in exactly the same situation and united in the same way . . . in a single prior art reference.'" *See Perkin-Elmer Corp. v. Computervision Corp.,* 221 USPQ 669, 673 (Fed. Cir. 1984). Furthermore, the court in *Ex Parte Lee* 31 USPQ2d 1105, 1110 (BPAI 1993), requires that an anticipatory reference under 35 USC §102 must be an identical disclosure "satisfying *each and every element* of the claimed invention" (emphasis added).

Appellant is aware that anticipation need not necessarily be stated or provided expressly since the courts have found that "Anticipation can occur when a claimed limitation is 'inherent' or otherwise implicit in the relevant reference. *See Standard Havens Products, Inc. v. Gencor Industries, Inc.,* 21 USPQ2d 1321, 1328 (Fed. Cir. 1991). The courts apply rigorous requirements to inherent anticipation, requiring that an element which is inherently asserted *must necessarily result* from the reference document. See for example *In re Oelrich and Divigard,* 212 USPQ 223, 326 (CCPA 1981) (emphasis in original):

> Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. If, however, the disclosure is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient.

As reasoned above, appellant believes that it is inappropriate to include the additional '972 steps of forming and etching a cap layer on the substrate in claim 1. The '972 patent therefore fails to meet the 35 USC §102 anticipation requirements such as those stated by the courts in *du Pont* "[A]ny degree of physical difference, however slight, invalidates claims of anticipation", *Perkin-Elmer* "[T]here is no anticipation 'unless all the elements are found in exactly the same situation and united in the same way . . . in a single prior art reference'.", and *Lee* requiring that the anticipatory reference must satisfy "each and every element of the claimed invention". Also, appellant respectfully submits that the elements of claim 1 do not necessarily result from the '972 teachings. The '972 teachings thus fail to meet the *In re Oelrich* requirements for inherent anticipation.

Additionally regarding claim 1, appellant believes that the limitations of clauses (b) and (f) of claim 1 are not disclosed in the '972 teachings, see Issue 2,A.

For the reasons stated above, appellant believes that claim 1 is not anticipated by Inohara et al. (U.S. Pat. No. 5,976,972). Appellant therefore believes that claim 1 is patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat No. 5,976,972).

B. Regarding claim 5. Independent method claim 5 includes each of the limitations recited in claim 1. Appellant believes that claim 1 is patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972) as reasoned above concerning claim 1. Appellant therefore believes that claim 5 is patentable under 35 USC §102(e).

Additionally, claim 5 includes the further limitations of having an interconnect line in the substrate, depositing the first layer on the interconnect line without interposing a material layer between the first dielectric layer and the substrate and etching a via hole through the first dielectric layer to the interconnect line. The '972 patent teaches forming a cap layer between a layer such as appellant's claimed first dielectric layer and the '972 lower wiring element such as appellant's first dielectric layer, and etching through the cap layer, see appellant's above argument regarding claim 1, Issue 4,A.

Claim 5 does not include the limitation including any layer that is formed between the substrate and the first dielectric layer. The '972 patent includes a cap layer interposed between the substrate and the first dielectric layer, and therefore fails to meet the 35 USC §102 anticipation requirement such as stated in *du Pont, Perkin-Elmer* and *Lee.*

Furthermore, regarding the claim 5 limitation, "wherein the first and third dielectric layers comprise materials having similar etching characteristics." The '972 patent teaches etching a wiring groove 46 and an opening region 51 in etch stop layer 44 and disclosing that "The etching progresses only through the opening region 41 overlapping the groove 46. Thus, a contact hole 48 reaching the stopper film 54 is formed along with the groove 46" (column 13, lines 29-46 and Figs. 29 and 30). The '972 patent discloses that the etching of the wiring groove 46 and the contact hole 48 is accomplished by RIE, but appellant has been unable to discern any '972 teachings indicating that the etching of wiring groove 46 and contact hole is accomplished in one continuous etching process or that Inohara et al. layers 44 and 45 employ materials having similar etching characteristics. The '972 patent merely teaches forming the groove and the hole through RIE etching, thus lacking the recited limitation of claim 5. Appellant therefore believes

that the '972 patent does not meet the requirements for anticipation, either explicitly or inherently, under 35 USC §102(e).

For the reasons stated above, appellant believes that claim 5 is not anticipated by the '972 patent. Appellant therefore believes that claim 5 is patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972).

C. Regarding claims 7, 8, 11 and 12. Claims 7, 8, 11 and 12 depend from claim 1. Appellant believes that claim 1 is patentable under 35 USC §102(e), see Issue 4,A. Appellant therefore believes that claims 7, 8, 11 and 12 are patentable under 35 USC 102(e) over Inohara et al. (U.S. Pat. No. 5,976,972).

Additionally regarding claim 11. Appellant notes that the via hole as recited in claim 1 forms the antecedent basis for the via hole as recited in claim 11. This via hole is etched through the first dielectric layer, thereby forming a via hole extending to the substrate (claim 1, clause (i)). The '972 patent teaches forming the via hole through a cap layer, as reasoned more fully in connection with claim 1, see Issue 4,A. Consequently, the '972 conductive material extends through a cap layer, while the conductive material recited in claim 11 does not extend through any layer interposed between appellant's first dielectric layer and the substrate. The '972 patent thus fails the identical disclosure requirement for a finding of 35 USC §102(e) anticipation.

For the reasons stated above, appellant believes that claims 7, 8, 11 and 12 are not anticipated by Inohara et al. (U.S. Pat. No. 5,976,972). Appellant therefore believes that claims 7, 8, 11 and 12 are patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972).

Issue 5 – Whether claims 13 and 16-18 are patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972)?

A. Regarding claim 13. Independent claim 13 includes the limitation of forming the first and second trenches such that the distance between the first and second trenches exceeds the width of the sacrificial etch segment. Appellant submits that the '972 patent teaches forming a sacrificial etch segment that equals the distance between the first and second trenches, see for example '972 Figs. 39 and 40. In connection with claim 14 (the limitation of claim 14 is presently incorporated in appealed claim 13), the Examiner stated as follows.

> With respect to claim 14, interpreting the claim under a broad scope, rejection is based on the scope that forming the first trench at a distance D from the second trench at a width W, such that D exceeds W by a measure N, the measure N is chosen to be zero (Examiner Detailed Action memorandum mailed 10/18/01, item 4 p. 4).

Regarding the ordinary and accustomed meaning of the term "exceeds", appellant makes reference to the dictionary meaning of this term, stating in part:

> **Exceed** . . . **vt** . . . **2** to be more than or greater than: surpass; outdo . . . (see Webster New World Dictionary, Third College Edition, Simon & Schuster, Inc., New York, New York, 1988, p. 473).

Appellant submits that the Examiner's interpretation of the term "exceeds" as including the measure zero, is inconsistent with the ordinary and accustomed meaning of this term. Appellant therefore believes that claim 13 is not anticipated by the '972 patent.

For the reasons provided above, appellant believes that claim 13 is patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972).

B. Regarding claims 16-18. Claims 16-18 depend from claim 13. Appellant believes that claim 13 is patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972), see above. Appellant therefore believes that claims 16-18 are patentable under 35 USC §102(e) over Inohara et al. (U.S. Pat. No. 5,976,972).

Issue 6 – Whether claims 13 and 16-18 are patentable under 35 USC §102(e) over Lin (U.S. Pat. No. 6,093,632)?

A. Regarding claim 13. Independent claim 13 recites the limitation that the widths of the first and second trenches is narrower than the width of the first and second via etch patterns respectively. Appellant submits that the '632 patent teaches forming via patterns 12a and 15b, see Figs. 5B and 5C, wherein the via patterns are narrower than the trench width. For example:

> Opening 12a, or the space between silicon nitride islands, which will subsequent translate to the diameter of the narrow diameter opening, of the dual damascene opening, is at least 500 Angstroms. (column 5, lines 39-43).

Furthermore, with reference to Figs. 5-8 see column 5 lines 56-61 as follows.

> A selective, first RIE cycle, using CH_3 as an etchant, creates wide opening 15b, in silicon oxide layer 13, using opening 15a, in photoresist shape 14, as a mask, while creating narrow diameter opening 12b, in second silicon oxide layer 4, using opening 12a, located between small area silicon nitride islands 10b, as a mask.

Appellant therefore believes that the '632 patent fails to meet the identical disclosure requirement for a finding of anticipation under 35 USC §102(e).

Additionally regarding claim 13. A review of '632 Fig. 6 shows that trench patterns 15 (layer 10a) are formed over the first and third openings 12b, but not over the center opening 12b. However, Figs. 7 and 8 show that center opening 12b has been widened to the same width as the adjacent trenches. Applicant respectfully submits that Fig. 6 is inconsistent with Figs. 7 and 8, with regard to the center opening, and is inconsistent with the text designating opening 12a as subsequently translating to the diameter of the narrow opening, of the dual damascene opening (column 5, lines 39-42). Appellant submits that these '632 inconsistencies between figures as well as between figures and the text show that the '632 teachings concerning Figs. 6, 7 and 8 do not provide an enabling disclosure with regard to openings 12a and 12b. A prior art disclosure providing anticipation "must be such as will give possession of the invention to the person of ordinary skill". *See Paperless Accounting v. Bay Area Rapid Transit System,* 231 USPQ 649, 653 (Fed. Cir. 1986). The court in *Paperless* also stated "even if the claimed invention is disclosed in a printed publication, that disclosure will not suffice as prior art if it was not enabling".

Also, concerning anticipation, see *Akzo N.V. v. U.S. International Trade Commission,* 1 USPQ2d 1241, 1245 (Fed. Cir. 1986). "[T]he prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public". Appellant respectfully submits that '632 Figs. 7 and 8 are not anticipatory with respect to openings 12a and 12b. Appellant therefore believes that claim 13 is not anticipated by the '632 patent.

As reasoned above, appellant believes that claim 13 is not anticipated by the '632 patent. Appellant therefore believes that claim 13 is patentable under 35 USC §102(e) over Lin (U.S. Pat. No. 6,093,632).

B. Regarding claims 16-18. Claims 16-18 depend from claim 13. Appellant believes that claim 13 is patentable under 35 USC §102(e) over Lin, as reasoned above. Appellant therefore believes that claims 16-18 are patentable under 35 USC §102(e) over Lin (U.S. Pat. No. 6,093,632).

Issue 7 – Whether claims 19, 23 and 28-30 are patentable under 35 USC §102(e) over Lin (U.S. Pat. No. 6,093,632)?

A. Regarding claim 19. Independent claim 19 includes the following limitations: (1) the widths of the first and second trenches is narrower than the width of the first and second via etch pattern respectively and (2) the distance between the first and second trenches exceeds the width of the sacrificial etch segment. The '632 patent teaches forming via patterns (12a) and trenches (15b), wherein the via pattern width is narrower than the trench width, as reasoned above in appellant's Issue 6,A regarding claim 13. Additionally, appellant believes that the '632 patent does not provide an enabling disclosure for forming sacrificial etch segments as reasoned above, see Issue 6,A regarding claim 13. Appellant therefore believes that the '632 patent fails to meet the identical disclosure and enabling disclosure requirements for a finding of anticipation under USC 35 §102(e).

Additionally regarding claim 19, appellant believes that limitations of clauses (b) and (f) are not disclosed in the '632 teachings, see Issue 2,D.

For the reasons stated above, appellant believes that claim 19 is not anticipated by the '632 patent. Appellant therefore believes that claim 19 is patentable under USC 35 §102(e) over Lin (U.S. Pat. No. 6,093,632).

B. Regarding claims 23 and 28-30. Claims 23 and 28-30 depend from claim 19. Appellant believes that claim 19 is patentable under USC 35 §102(e) over Lin, as reasoned above. Appellant therefore believes that claims 23 and 28-30 are patentable under USC 35 §102(e) over Lin (U.S. Pat. No. 6,093,632).

Issue 8 – Whether claim 11 is patentable under 35 USC §112, second paragraph?

Dependent claim 11, as provided in the proposed amendment, includes the limitation wherein "the trench" as filed is recited as "the second trench" for which the antecedent basis is recited in base claim 1 (j). Appellant believes that "the second trench" as recited in the amendment, claims the subject matter distinctly, thus meeting the requirements of 35 USC §112, second paragraph. Appellant therefore believes that claim 11 is patentable under 35 USC §112, second paragraph.

Issue 9 – Whether the proposed amendments of claims 5, 11-13, 15, 19 and 24 raise new issues that require further search/consideration?

A. Regarding claim 5. Independent claim 5 is amended to include the limitations of claim 1 and additionally reciting "depositing a first dielectric layer on the substrate such that there is no material layer interposed between the interconnect line and the substrate" (clause a). Appellant submits that this limitation is not new since it is the same as the limitation in claim 1 wherein the term "on" precludes depositing a layer between the first dielectric layer and the substrate as argued above in Issue 4,A regarding claim 1. Appellant therefore believes that the amendment to claim 5 does not raise new issues.

B. Regarding claim 11. Dependent claim 11 is amended by changing the expression "the trench" to "the second trench". The antecedent base for "the trench" is "the second trench" as recited in base claim 1 (j). Appellant therefore believes that the amendment to claim 11 does not raise new issues.

C. Regarding claim 12. Dependent claim 12 has been amended to limit metallic superconductors and nonmetallic superconductors to conductive materials "having zero direct current resistance at or below their superconducting transition temperature". The limitation "metallic superconductors and nonmetallic superconductors" was recited in claim 12 as filed. Appellant believes that the additional limitation recited in the amendment to claim 12 merely states the commonly accepted definition of the term superconductors (as provided in the specification at page 23, lines 9-12) see for example:

> **SUPERCONDUCTOR.** The most spectacular property of a superconductor is the total disappearance of its electrical resistance when it is cooled below a critical temperature T_c (Van Nostrand's Scientific Encyclopedia, 5th Ed., Van Nostrand Reinhold Company, New York, New York, p. 2128, 1976)

Furthermore see:

> **Superconductivity** . . . The temperature at which the transition occurs is called the transition or critical temperature T_c (McGraw-Hill Concise Encyclopedia of Science & Technology, 3rd. Ed., McGraw-Hill, Inc. New York, New York, p. 1842, 1994).

Appellant therefore believes that the amendment to claim 12 does not raise new issues.

D. Regarding claim 13. Independent claim 13 is amended to include the limitations (1) extending the first and second via patterns through the etch stop layer, (2) the distance between the first and second trenches exceeds the width of the sacrificial etch segment and (3) the widths of the first and second trench are narrower than the width of the first and second via etch patterns respectively. Regarding the claim 13 limitation of etching the first and second via patterns through the etch stop layer. Appellant believes that this limitation was provided in claim 13 as provided in appellant's 6/29/01 Amendment and

Response in response to the First Office Action Mailed 1/10/01 "anisotropically etching the first and second via patterns through the etch stop layer" (claim 13 (c), p.3). Regarding the claim 13 limitation concerning the distance between the first and second trenches exceeding the width of the sacrificial etch segment. This limitation was provided in claim 14 as filed wherein the term "exceeds" does not include the value/measure zero, see Issue 5,A. Regarding the claim 13 limitation wherein the width of a trench is narrower than the width of the corresponding via patterns. This limitation was provided in claim 1 as filed. For the reasons provided above, appellant believes that the amendment to claim 13 does not raise new issues.

E. Regarding claim 15. Dependent claim 15 is amended to include the limitation wherein the distance between the first and second trenches exceeds the width of the sacrificial etch segment by at least 0.02μ. Appellant believes that this limitation was provided in claims 13-15 as filed. Appellant therefore believes that the amendment to claim 14 does not raise new issues.

G. Regarding claim 19. Independent claim 19 is amended to include the limitations wherein (1) the width of the first and second trenches is narrower than the width of the respective via patterns and (2) the distance between the first and second trenches exceeds the width of the sacrificial etch segment. Appellant believes that these limitations were provided in claims 1, 13 and 14 as filed, see also Issue 9,D concerning claim 13. Appellant therefore believes that the amendment to claim 19 does not raise new issues.

H. Regarding claim 24. Dependent claim 24 is amended to include the limitation wherein the distance between the first and second trench patterns exceeds the width of the sacrificial etch segments by at least 0.02μ. Appellant believes that this limitation was provided by claims 19 and 24 as filed and wherein the term "exceeds" does not include the value/measure zero, see Issue 5,A. Appellant therefore believes that claim 24 does not raise new issues.

Appendix A

Following are the claims on appeal.

1. A method of forming a structure on a substrate, the method comprising:
   a) depositing a first dielectric layer on the substrate;
   b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics;
   c) depositing a first mask layer on the second dielectric layer, wherein the first mask layer includes a first via pattern having a width T;
   d) anisotropically etching the first via pattern through the second dielectric layer;
   e) removing the first etch mask;
   f) depositing a third dielectric layer on the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics;
   g) depositing a second mask layer on the third dielectric layer, wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P, such that T exceeds P by a measure M;
   h) anisotropically etching the trench pattern through the third dielectric layer, thereby forming (1) a first trench in the third dielectric layer and (2) a second via pattern;
   i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the substrate; and
   j) anisotropically etching the first trench through the second dielectric layer, thereby forming a second trench extending through the second and third dielectric layers, wherein the via hole and second trench are adapted for fabricating a dual damascene structure.

5. A method of forming a structure on a substrate including at least one interconnect line, the method comprising:

a) depositing a first dielectric layer on the substrate such that there is no material layer interposed between the interconnect line and the substrate;

b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics;

c) depositing a first mask layer on the second dielectric layer, wherein the first mask layer includes a first via pattern having a width T;

d) anisotropically etching the first via pattern through the second dielectric layer;

e) removing the first etch mask;

f) depositing a third dielectric layer on the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics and wherein the first and third dielectric layers comprise materials having similar etching characteristics;

g) depositing a second mask layer on the third dielectric layer, wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P, such that T exceeds P;

h) anisotropically etching the trench pattern through the third dielectric layer, thereby forming (1) a first trench in the third dielectric layer and (2) a second via pattern;

i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the interconnect line; and

j) anisotropically etching the first trench through the second dielectric layer, thereby forming a second trench extending through the second and third dielectric layers, wherein the via hole and second trench are adapted for fabricating a dual damascene structure.

6. The method of claim 1 wherein M is at least 0.02μ.

7. The method of claim 1 wherein the first and third dielectric layers comprise one or more dielectric materials selected from the group consisting of amorphous fluorinated carbon, organic spin-on materials, spin-on glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers and divinyl siloxane benzocyclobutane.

8. The method of claim 7 wherein the second dielectric layer comprises one or more dielectric materials selected from the group consisting of silicon oxides, silicon nitrides and silicon carbides.

9. The method of claim 1 wherein depositing a first mask layer comprises depositing a mask layer selected from the group consisting of photoresist mask layers, hard mask layers and combinations of photoresist mask layers and hard mask layers.

10. The method of claim 1 wherein the first and third dielectric layers comprise Black Diamond™.

11. The method of claim 1 additionally comprising simultaneously filling the second trench and the via hole with a conductive material, whereby a dual damascene structure is formed.

12. (once amended) The method of claim 11 wherein the conductive material comprises one or more materials selected from the group consisting of metallic superconductors and nonmetallic superconductors having zero direct current resistance at or below their superconducting transition temperature.

13. A method of forming a structure on a substrate, the method comprising:

a) forming a dielectric stack including an etch stop layer;

b) depositing a first mask layer on the etch stop layer wherein the first mask includes: (1) a first via pattern having a width WV1, (2) a second via pattern having a width WV2 and (3) a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS;

c) anisotropically etching the first and second via patterns through the etch stop layer thereby extending the first and second via patterns through the etch stop layer and forming a sacrificial etch segment by anisotropically etching the sacrificial etch pattern through the etch stop layer;

d) forming a first trench on the etch stop layer such that the first trench does not overlay the sacrificial etch segment and wherein the first trench has a width WT1 that is narrower than WV1;

e) forming a second trench having a width WT2 on the etch stop layer, such that (1) the second trench does not overlay the sacrificial etch segment, (2) the sacrificial etch segment is positioned between the first and second trenches, (3) the distance between the first and second trench exceeds WS and (4) WT2 is narrower than WV2;

f) forming a first via hole underlying the first trench, such that the first via hole communicates with the first trench and with the first via pattern extending through the etch stop layer; and

g) forming a second via hole underlying the second trench, such that the second via hole communicates with the second trench and with the second via pattern extending through the etch stop layer, wherein: (1) the first trench and the first via hole, and (2) the second trench and the second via hole area adapted for forming a first dual damascene structure and a second dual damascene structure respectively.

15. The method of claim 13 wherein the distance between the first and second trenches exceeds WS by at least 0.02μ.

16. The method of claim 13 wherein the etch stop layer comprises one or more dielectric materials selected from the group consisting of silicon oxides, silicon nitrides and silicon carbides.

17. The method of claim 13 additionally comprising simultaneously filling the first and second trenches, and the first and second via holes with a conductive material, whereby first and second dual damascene structures are formed.

18. The method of claim 17 wherein the conductive material comprises one or more materials selected from the group consisting of metals, alloys, metallic superconductors and nonmetallic superconductors.

19. A method of forming a structure on a substrate, the method comprising:

a) depositing a first dielectric layer on the substrate;

b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics;

c) depositing a first mask layer on the second dielectric layer wherein the first mask includes: (1) a first via pattern having a width WV1, (2) a second via pattern having a width WV2 and (3) a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS;

d) anisotropically etching the first and second via patterns through the second dielectric layer and forming a sacrificial etch segment by simultaneously anisotropically etching the sacrificial etch pattern through the second dielectric layer;

e) removing the first mask layer;

f) depositing a third dielectric layer on the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics;

g) depositing a second mask layer on the third dielectric layer, wherein the second mask layer includes: (1) a first trench pattern overlaying the first via pattern and the third dielectric layer, and having a width WT1 and (2) a second trench pattern having a width WT2 overlaying the second via pattern and the third dielectric layer, and having a distance D between the first and second trench patterns wherein D exceeds WS;

h) anisotropically etching the first and second trench patterns through the third dielectric layer, thereby forming a first trench and a second trench, additionally forming a third and a fourth via pattern; and

i) anisotropically etching the third and fourth via patterns through the first dielectric layer, thereby forming a first via hole and a second via hole, wherein (1) the first trench and the first via hole are adapted for forming a first dual damascene structure and (2) the second trench and second via hole are adapted for forming a second dual damascene structure.

23. The method of claim 19 wherein the first and third dielectric layers comprise materials having similar etching characteristics.

24. The method of claim 19 wherein D exceeds WS by at least 0.02μ.

25. The method of claim 19 wherein the first and third dielectric layers comprise one or more dielectric materials selected from the group consisting of amorphous fluorinated carbon, organic spin-on materials, spin-on glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers and divinyl siloxane benzocyclobutane.

26. The method of claim 25 wherein the second dielectric layer comprises one or more dielectric materials selected from the group consisting of silicon oxides, silicon nitrides and silicon carbides.

27. The method of claim 19 wherein the first and third dielectric layers comprise Black Diamond™.

28. The method of claim 19 wherein depositing a first mask layer comprises depositing a mask layer selected from the group consisting of photoresist mask layers, hard mask layers and combinations of photoresist layers and hard mask layers.

29. The method of claim 19 additionally comprising simultaneously filling: (1) the first trench and the first via hole, and (2) the second trench and the second via hole with a conductive material, whereby first and second dual damascene structures are formed.

30. The method of claim 29 wherein the conductive material comprises one or more materials selected from the group consisting of metals, alloys, metallic superconductors and nonmetallic superconductors.

Respectfully submitted,

Dated: August 1, 2002

By: _____

Albert J. Dalhuisen

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